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POWER THE FUTURE

AN004

Application Note

LV InnoGaN Parallel Design Guide

Content

1 Why Paralleling

Due to the continuously increase of power rating, lower on-state resistance RDS(on) is needed for switching transistors. In many applications, one single switching transistors is no longer sufficient for the current capability of the system. Thus parallel connection of multi- devices is needed to reduce the conduction losses and device temperatures, and meanwhile increase the efficiency of power converters. However, engineers have to deal with the issues of imbalanced current and power loss sharing among the paralleled devices due to the sightly asynchronous conduction and turn-on/turn-off processes.

2 Characteristics of Paralleled LV InnoGaN

In this appication note, the reason of why HV InnoGaN is suitable for parallelling in low power applications will be demonstrated from the aspects of $V_{GS(th)}$, $R_{DS(on)}$, and Gm.

2.1 Threshold Voltage - $V_{GS(th)}$

For power devices, $V_{GS(th)}$ represents the turn-on threshold voltage . The device stops conducting current when the gate driving voltage is below the threshold voltage. For GaN power devices, the threshold voltage is the voltage at which the 2-dimensional electron gas (2DEG) beneath the gate is completely depleted. When multiple GaN devices are paralleled, the relationship between $V_{GS(th)}$ and T_J (junction temperature) needs to be considered.

A buck converter with four paralleled InnoGaN devices is taken as an example for simulation. to analize the current sharing performance between GaN devices with different $V_{GS(th)}$ during turn-on and turn-off processes.

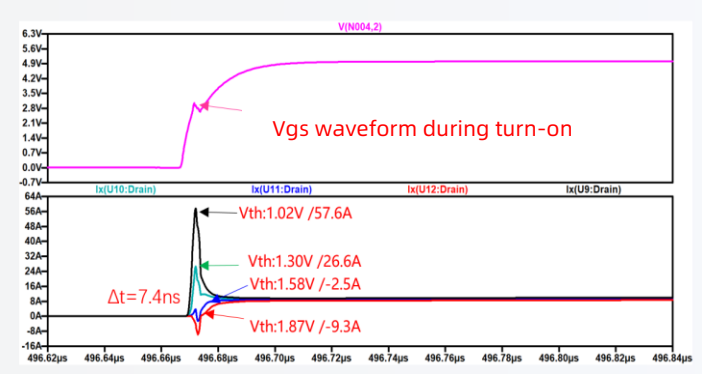


Figure 1 Current sharing during turn-on process

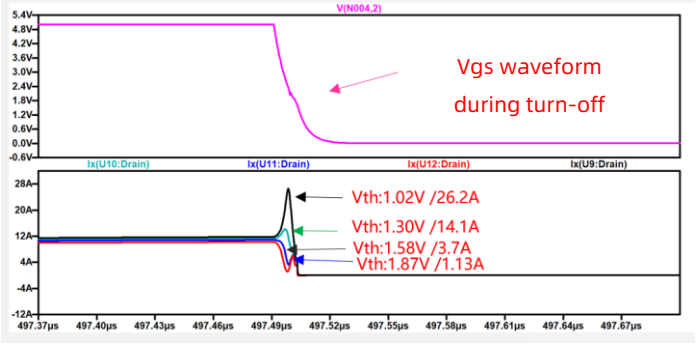


Figure 2 Current sharing during turn-off process

It is observed from the simulation results that higher current flows through the device with smaller threshold voltage ($V_{GS(th)}$) during both turn-on and turn-off processes, resulting in higher switching losses.

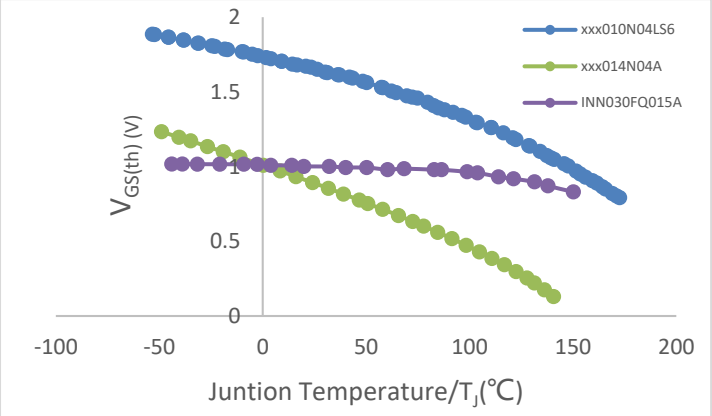


Figure 3 The relationship between $V_{GS(th)}$ and T_J

Based on the relationship between $V_{GS(th)}$ and T_J as mentioned above, it could be concluded that T_j has high significant influence on $V_{GS(th)}$ for Si power devices. Devices with lower threshold voltages suffer from increased turn-on/turn-off losses, leading to higher overall losses. Then with increased T_J, decreased $V_{GS(th)}$ resulting in even higher current flow and losses, which exacerbats the unbalanced current sharing and is unsuitable for parallelling. However, the $V_{GS(th)}$ of LV InnoGaN is relatively stable with to the variation of T_J, which benifits parallelling application.

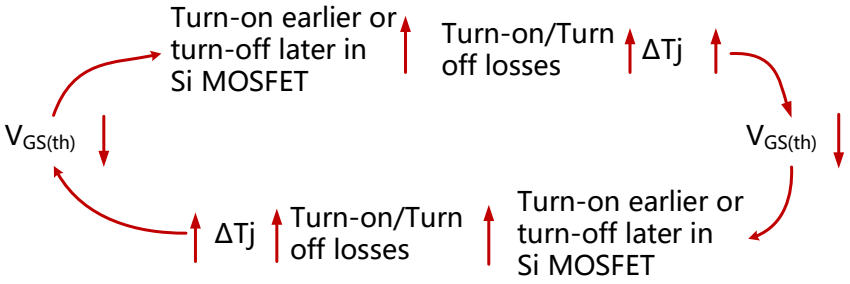


Figure 4 The relationship between $V_{GS(th)}$ and T_J for Si devices when paralleled

2.2 On-State Resistance - $R_{DS\ (on)}$

The on-state resistance, $R_{DS(on)}$, refers to the sum of all resistances within the device. When paralleled GaN devices are in on-state, smaller $R_{DS(on)}$ results in a higher current, while larger $R_{DS(on)}$ leads to a lower current on the contrary.

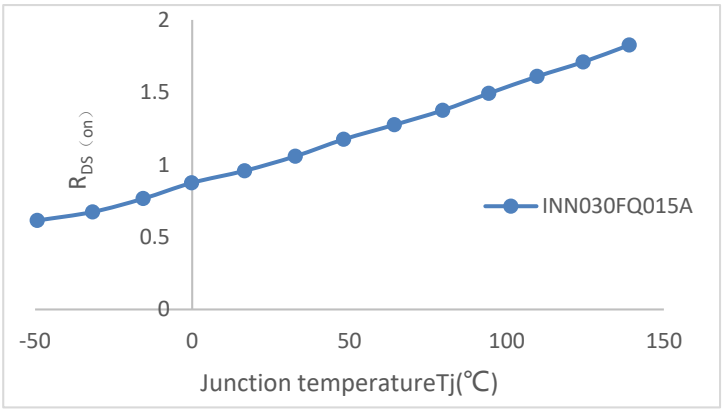


Figure 5 The relationship between $R_{DS(on)}$ and TJ

The relationship between $R_{DS(on)}$ and T_J shown as above in Figure 5. The temperature coefficient between $R_{DS(on)}$ and T_J is positive, which means that $R_{DS(on)}$ increases with T_J, Based on the equation P=(U^2)/($R_{DS(on)}$), it can be deduced that the conduction loss increases with a lower T_J. Then $R_{DS(on)}$ of the device increases and pwer loss decreases when T_J rises, forming a negative feedback and eventually balanced current sharing.

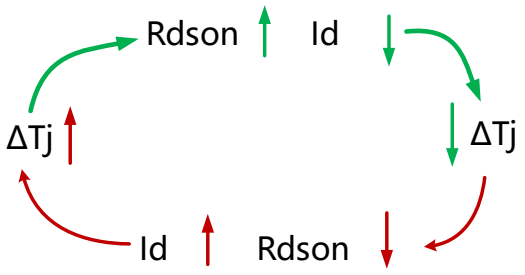


Figure 6 The relationship between $R_{DS(on)}$ and T_J for LV InnoGaN

2.3 Transconductance - Gm

The transconductance Gm represents the control of Vgs voltage to the channel current, which could be expressed as follows:

$$Gm = \frac{\Delta Id}{\Delta Vgs}$$

With the same ΔVgs, a larger Gm corresponds to a larger current flowing through the channel.

Simulation results are obtained to show the current distribution in a Boost converter with three GaN devices in parallel and with different Gm. The simulation results are shown as follows:

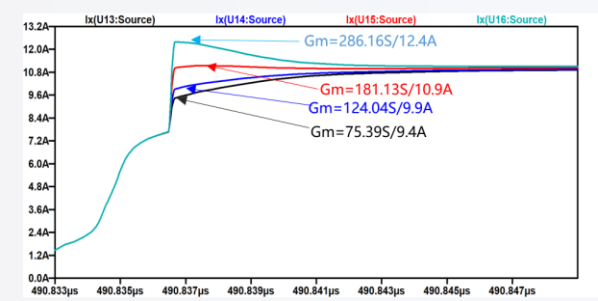


Figure 7 The current distribution of different Gm during turn-on

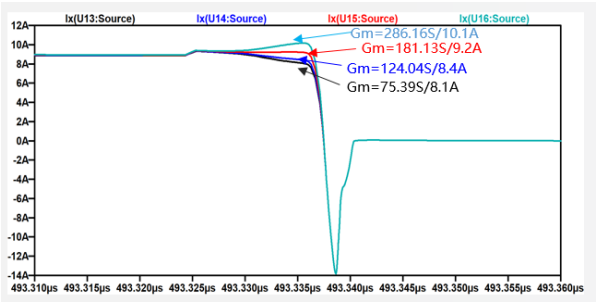


Figure 8 The current distribution of different Gm during turn-off

The simulation results indicates that larger Gm leads to higher current passing through the devices during turn-on and turn-off processes. This is because a larger Gm results in a higher current capability during both turn-on and turn-off transents, and thus the switching losses are higher.

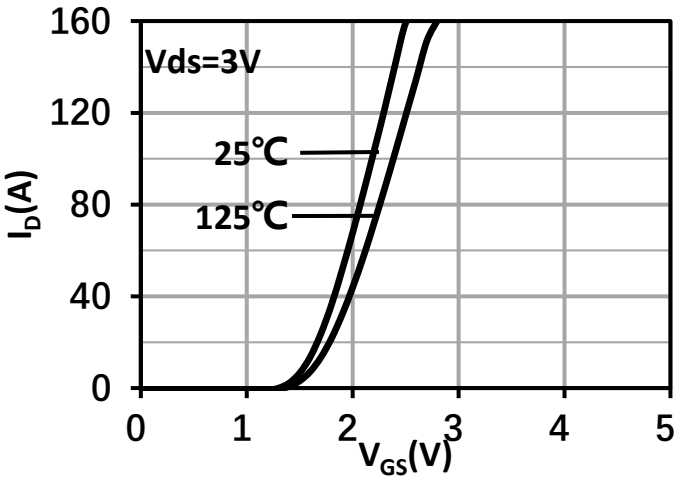


Figure 9 The transfer characteristics of INN030FQ015A at different temperature

The transfer curves for LV InnoGaN INN030FQ015A are shown in Figure 9, The curves indicate that the transconductance (Gm) is 71S at 25°C and while decreases to 42S at 125°C where Gm decreases gradually as TJ increases. The devices with higher Gm conduct a greater portion of the turn-on and turn-off

current when paralleled, leading to the increase of switching losses and overall device losses. However, Gm decreases with increased TJ, resulting in a reduction of the currents sharing and decreased losses. This will eventually form a balanced status between paralleled devices.

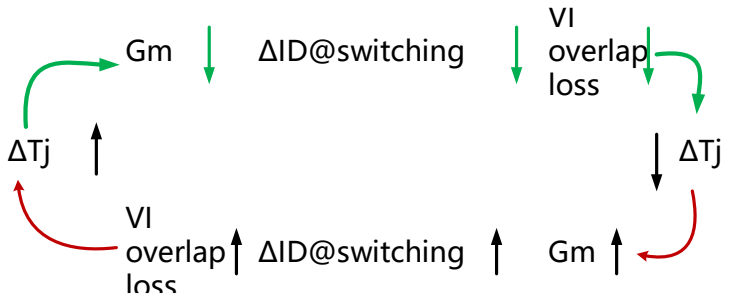


Figure 10 The relationship between Gm and TJ of paralleled InnoGaN

2.4 Summary

After analyzing the feasibility of parallel connection based on $V_{GS(th)}$, $R_{DS(on)}$, and Gm of InnoGaN, it is concluded that InnoGaN is suitable for parallelling applications. To ensure the feasibility of paralleled InnoGaN, specific considerations should be addressed when designing the gate driving loops and power loops. ,

3 Layout Design of Paralleled InnoGaN

3.1 PCB layout Design Considerations

In order to achieve higher power , multiple GaN devices need to design in parallel in some applications require the use of . This section will discuss the design methods for paralleled multiple GaN devices to achieve performance consistency from the aspects of common-source inductance, power loop, and driving loop designs.

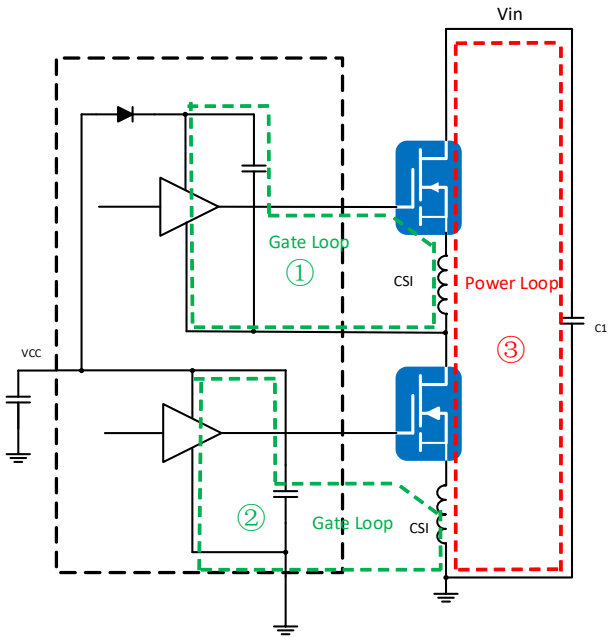


Figure 11 Half-bridge power loop schematic

3.1.1 Common-Source Inductance

Common Source Inductor (CSI) is the common part that gate driving circuit and the power circuit shared at the source terminal of the GaN device as shown in Figure 11.

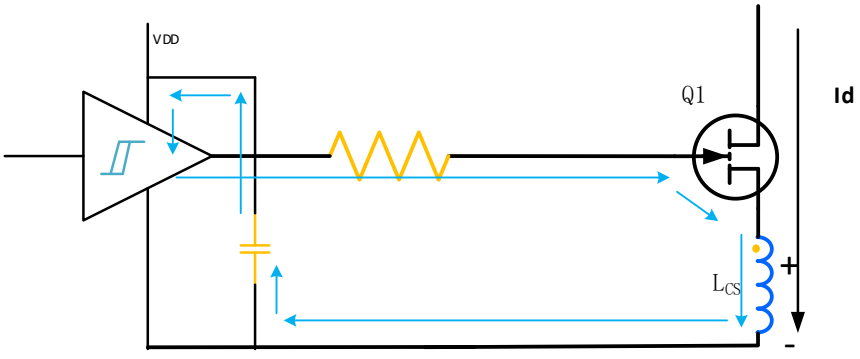


Figure 12 The common-source inductor in the circuit

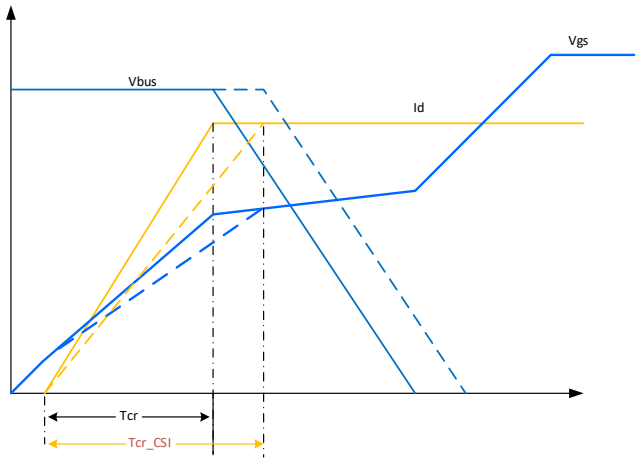


Figure 13 The impact of common-source inductor

During the device turn-on process, the value of di/dt depends on the pull-up/pull-down capability of the driving circuit. With the common source inductor, the drain current slew rate di/dt will generate a negative voltage across the common source inductor during the turn-on process. Therefore the current that charges the gate capacitance is reduced, leads to extended transition time Tcr, increased turn-on losses, and lower efficiency. Attention should be paid to the common source inductor in paralleled InnoGaN design.

3.1.2 Power loop

Reducing parasitic inductance is crucial for the layout design of high-frequency power devices. The recommended PCB layout design method is as follows:

1.Place MLCC close to the high side InnoGaN. Use the top layer as the power loop forward path while the first inner layer as return path to form the smallest loop size. By this design approach the magnetic fields self-cancellationcould reduce the parasitic inductance in the power loop and benifit to reduce the voltage spikes and improve power efficiency.

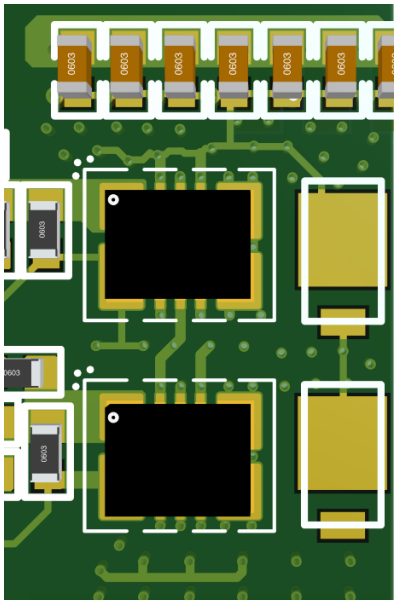


Figure 14 The top view of recommended PCB layout(1)

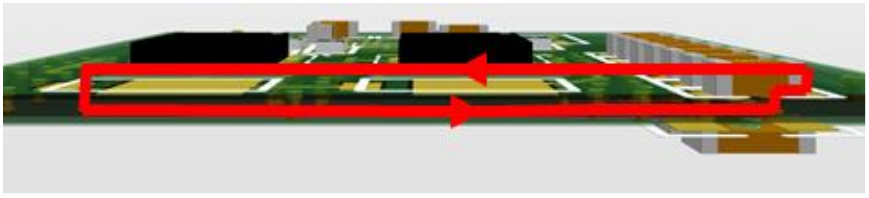


Figure 15 The cross section of recommended PCB layout(1)

Using interleaved vias for Drain and Source terminals. Interleaved vias with opposite current can reduce magnetic energy storage, which helps in magnetic field cancellationand reduce the eddy current and proximity effects, and minimize AC conduction losses.

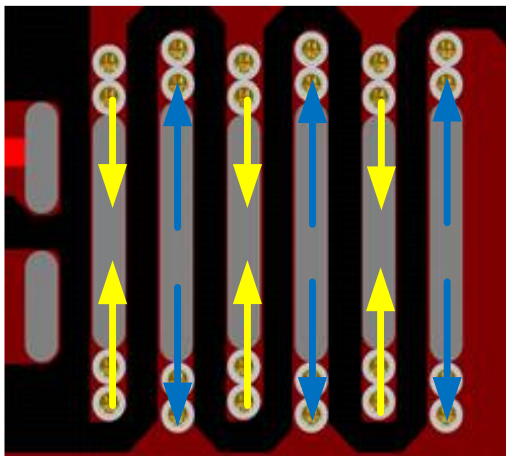


Figure 16 The top view of recommended PCB layout(2)

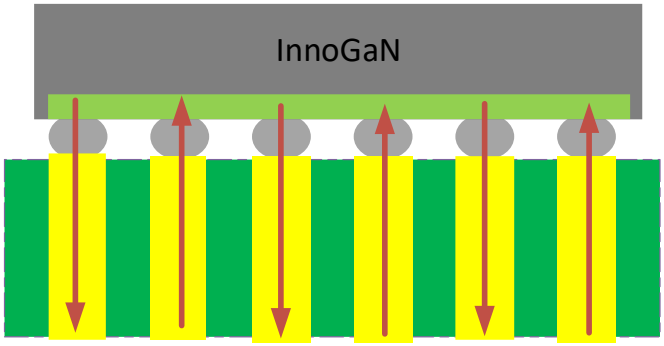


Figure 17 The cross section of recommended PCB layout(2)

3.1.3 Gate Driving Loop

Based on the driving design guide provided in 'AN002-LV InnoGaN Gate Driving Design Guide', R1, R2 and R3 are employed as the turn- on gate resistor , while R2, R3 also serve as the turn-off resistor . R2, R3, C1, and C2 should be placed as close as possible to the gate terminals in the layout design to suppress the ringing and voltage spike issues caused by long gate driving loop. Additionally, the Kelvin source design separates the gate driving loop and the power loop and reduces the effects of CSI (Common Source Inductance)effectively.

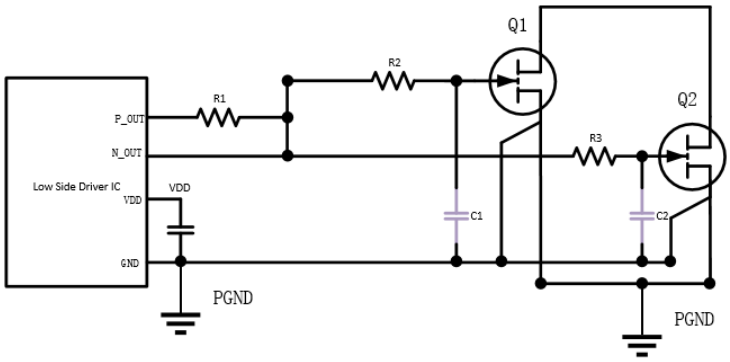


Figure 18 Driving design for paralleled InnoGaN

3.2 Paralleled InnoGaN Design

3.2.1 Parallel InnoGaN Design in Single-FET Topology

Applying paralleled multiple devices in singleFET topologies introduces complexity to the system layout when taken various current paths of each devices into consideration.

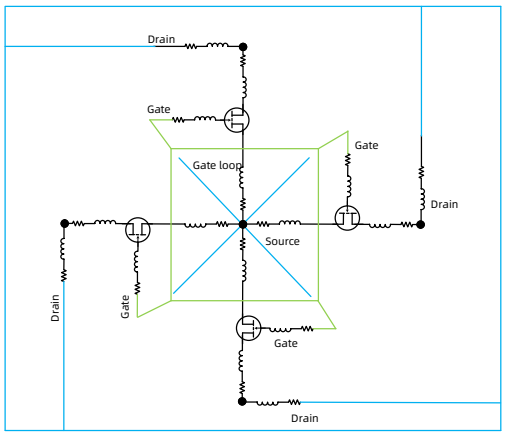


Figure 19 Symmetry layout diagram (Suitable for high-speed switching application)

To meet the requirement of symmetry layout of GaN devices, an design example is shown in Figure 12 with the symmetry of the power loop, the common source inductance (CSI), and gate driving loops. As the number of paralleled GaN devices increases, complete symmetry in the layout becomes more difficult to achieve. Therefore, priority should be given as follows:

1、 Symmetry in the Common-Source Inductance.

2、 Power loop.

3、 Gate driving loop.

3.2.2 Paralleled InnoGaN Design in Half-Bridge Topology

Although the layout method for single-FET topologies is also appliable, it may not be the most optimal layout solution for half-bridge topologies. The recommended solution is the mirror symmetry methodas shown in Figure 15.

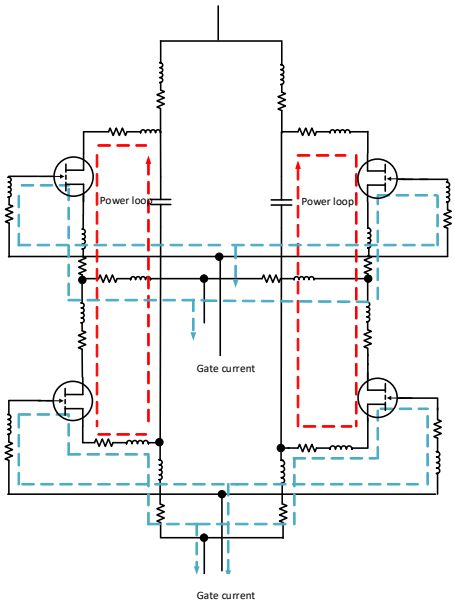


Figure 20 Half-bridge symmetry layout diagram

The symmetrical scheme realizes a reliable parallel connection for multiple GaN devices in half-bridge topoligies. It features independent power loops, which not only reduce the total loop parasitic parameters but also ensure the consistency of each parasitic parameters, providing the most balanced performance of each device.

4 Design Examples of Paralleled LV InnoGaN

4.1 Paralleled LV InnoGaN Design in half-bridge type Buck Circuit

Based on the design considerations in the previous sections, the symmetric parallel layout configuration as shown in Figure 22 is adopted in a Buck converter (half-bridge type) as a design case. This design case utilizes 4 piece of LV InnoGaN INN030FQ015A in parallel with a switching frequency of 300kHz.

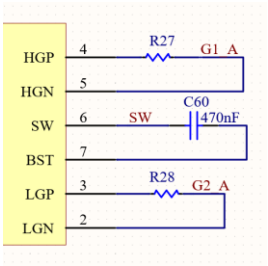


Figure 21 The gate driving circuit

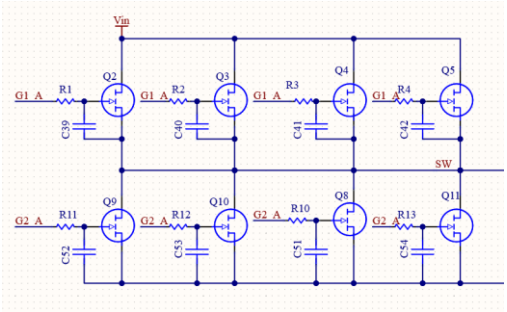


Figure 22 The symmetric schematic

The gate driving traces are relatively longer in the multiple-deviceparalleled applications than that of non-paralleled applications, Therefore, the gate resistors R1/R2/R3/R4/R10/R11/R12/R13 are recommended to be placed close to each GaN devices, to suppress the ringing caused by long gate driving loop. Additionally, Vgs oscillations could be further suppressed by placing capacitors between the Gate and Source terminals of the GaN devices without the compromise of switching speed. R27 and R28 are employed in this case to modify the turn-on and turn-off speed independently.

4.2 PCB Layout Design

The PCB layout designs in this case are shown as follows:

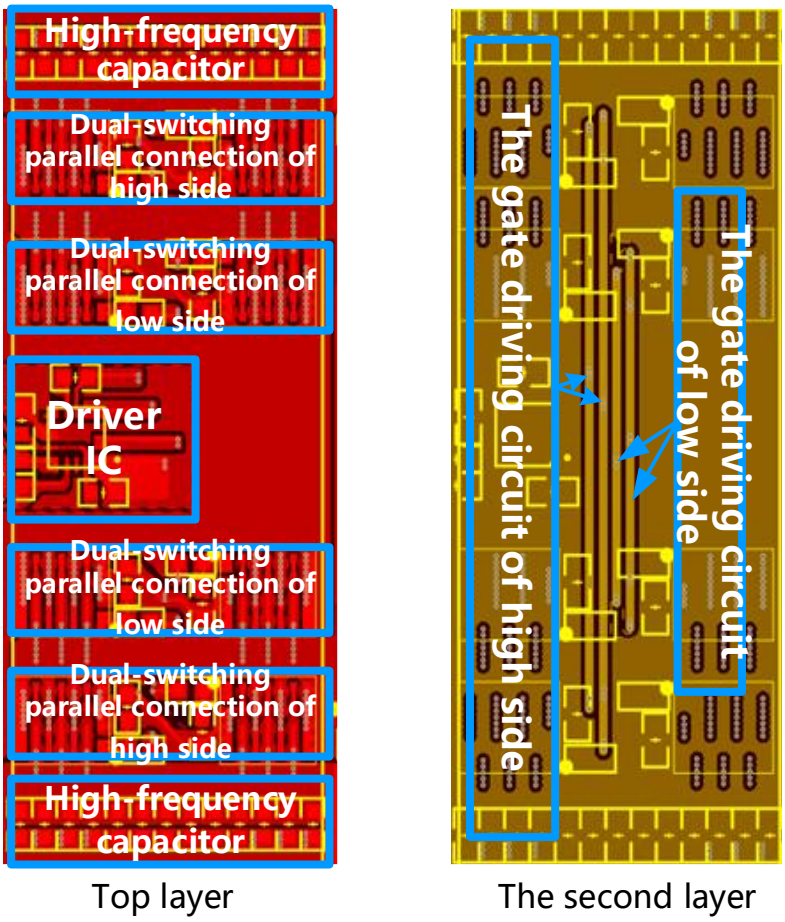


Figure 23 PCB layout of Buck circuit with 4 pieces of LV InnoGaN in parallel(1)

It could be seen from the top layer that the PCB layout design features symmetry with the driving IC as a midpoint both in ensuring vertical and horizontal directions. Additionally, each half-bridge cell is equipped with a set of high-frequency MLCC capacitors, which could reduce the parasitic parameters power effectively. The gate driving traces between different layers are connected with vias to minimize common-source inductance while ensuring gate driving loop symmetry. Moreover, the high-frequency loop are formed by the traces in top layer and power ground copper in the second layer as an optized high-frequency loop layout.

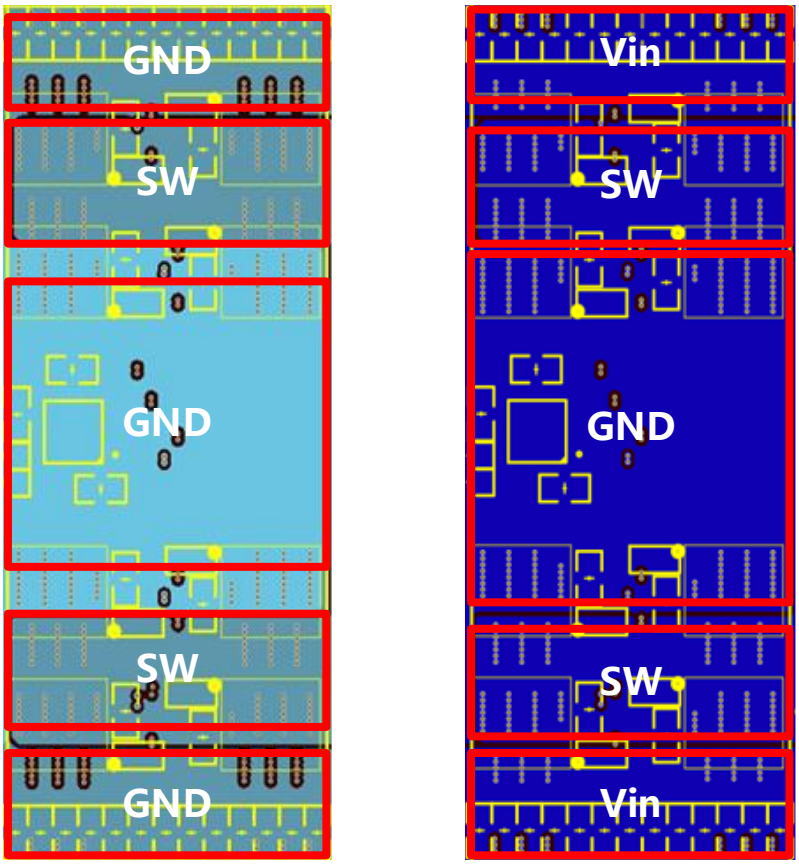


Figure 24 PCB layout of Buck circuit with 4 pieces of LV InnoGaN in parallel (2)

The third layer and bottom layer are the main current paths and heat dissipation paths, and need sufficient area for these functions.

5 Test Results

The evaluation board adopts a Buck circuit with 4 piece of LV InnoGaN in parallel. The specific layout is as follows: T1/T2/T3/T4 are the paralleled Buck active devices, while SR1/SR2/SR3/SR4 are the paralleled synchronous rectification devices.

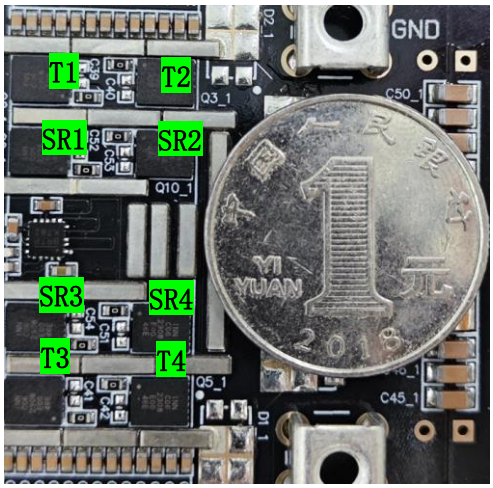


Figure 25 The design example of compact buck with 4 piece of LV InnoGaN in parallel

5.1 Gate driving waveforms

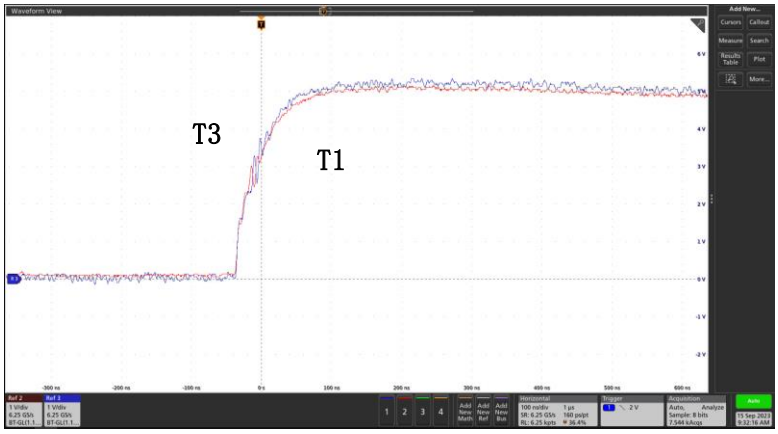


Figure 26 Comparison of gate to source voltage Vgs between paralleled GaN devices -

It could be concluded from Figure 26 that the Vgs transition process are almost identical for each GaN devices. These waveforms verify that symmetrical layout method benefits to balance the parasitic inductance, therefore providing better current sharing performance.

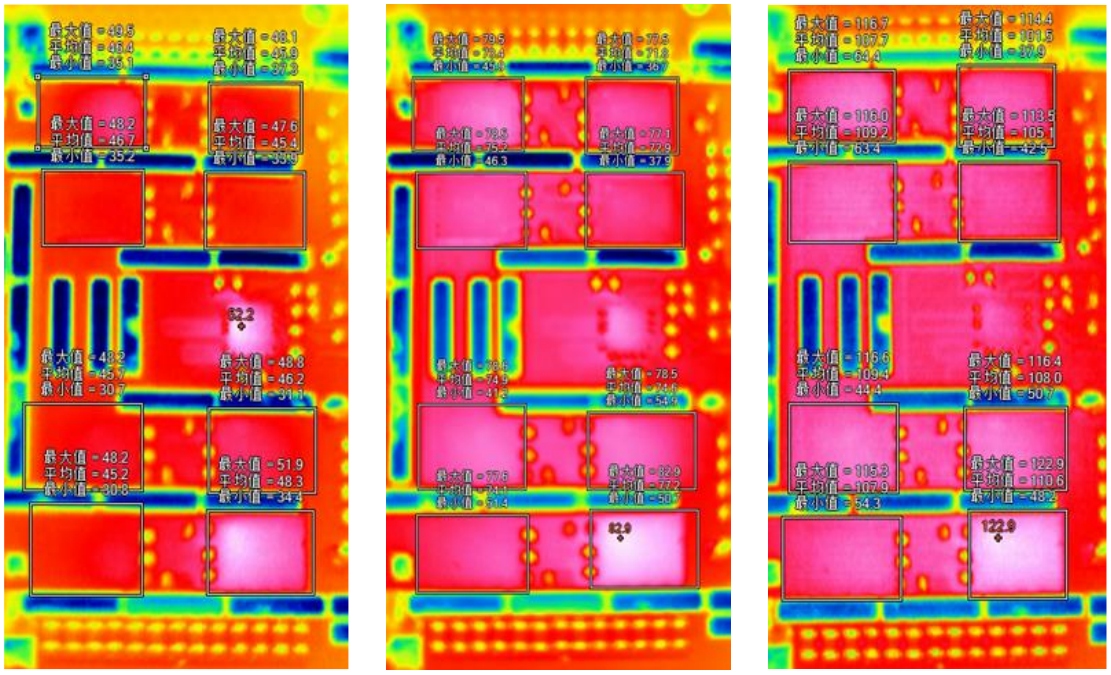
5.2 Thermal test results

This section focused on the thermal testing with the comparison of different conditions such as no airflow, with airflow, and with Heatsink for enhanced dissipation. The tests aim to evaluate the performance of the 4-device paralleled system's heat distribution. If the temperature variation between paralleled devices is less than 10°C, the current sharing performance is considered effective; On the contrary, the performance is considered below expectation when the temperature variation is greater than 10°C.

5.2.1 Without-airflow

Test condition: Vin=12V,Vout=5V,Fs=300kHz.

The hotspot temperatures are recorded and compared at the load current of 25A, 50A and 70A after 30 mins operation.



Iout:25A *Iout:50A* *Iout:70A*

Figure 27 Comparison of hotspot temperature at no-airflow and different current load

Table 1 Comparison of hotspot temperature with no-airflow and different current load

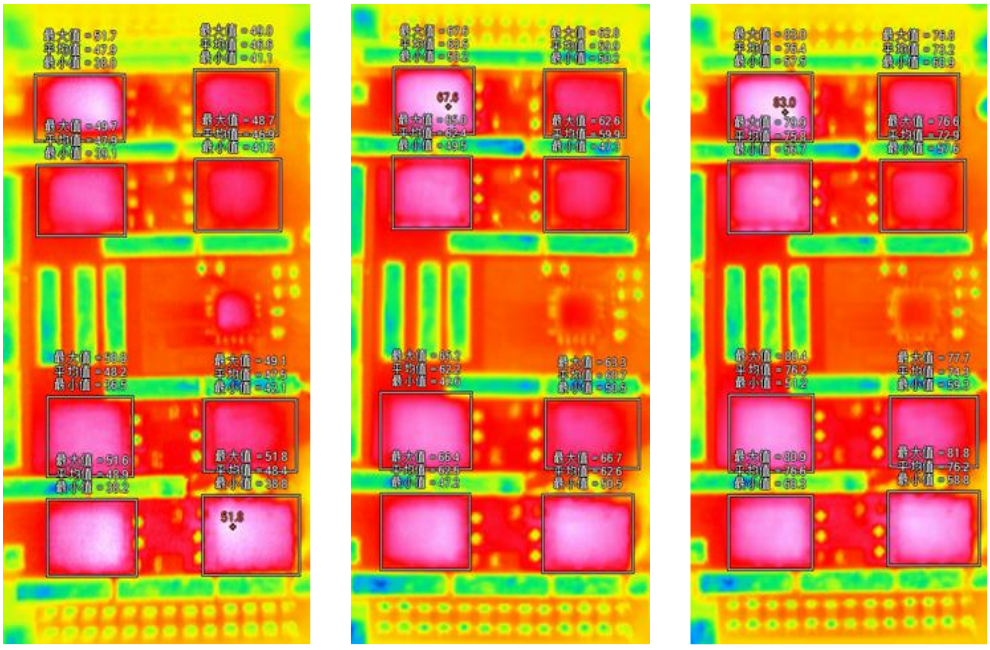
Iout	T1(℃)	T2(℃)	T3(℃)	T4(℃)	Temperature variation(℃)	SR1(℃)	SR2(℃)	SR3(℃)	SR4(℃)	Temperature variation (℃)
25A	49.5	48.1	48.2	51.9	3.8	48.2	47.6	48.2	48.8	1.2
50A	79.5	77.5	77.6	82.9	5.4	78.5	77.1	78.6	78.5	1.5
70A	116.7	114.4	115.3	122.9	8.5	116	113.5	116.6	116.4	2.9

The temperature variation between paralleled active GaN device is 8.5°C at 70A load current without airflow, while that between paralleled passive GaN device is 2.9°C. This indicates that good current sharing performance is achieved of paralleled devices. As the load increases, the temperature variation also increases. Therefore, , additional heat dissipation approaches are also required for higher power levels to ensure reliable parallel operation.

5.2.2 With Airflow and heatsink

Test condition: Vin=12V,Vout=5V,Fs=300kHz, with airflow of 3m/s.

The heatsink is mounted on the bottom side of the PCB. The hotspot temperatures are recorded and compared at the load current of 75A, 100A and 120A after 30 mins operation.



Iout:75A *Iout:100A* *Iout:120A*

Figure 28 Comparison of temperature variation at different current load with heatsink on bottom side

Table 2 Comparison of temperature variation at different current load with heatsink on bottom

Iout	T1(℃)	T2(℃)	T3(℃)	T4(℃)	Temperature variation (℃)	SR1(℃)	SR2(℃)	SR3(℃)	SR4(℃)	Temperature variation (℃)
75A	51.7	49	51.6	51.8	2.8	49.7	48.7	50	49.1	1.3
100A	67.6	62.8	66.4	66.7	4.8	65	62.6	65.2	63.3	2.6
120A	83	76.8	80.9	81.8	6.2	79.9	76.6	80.4	77.7	3.8

The temperature variation between paralleled active GaN device is 6.2°C with airflow and heatsink at the load current of 120A, while that of the passive paralleled GaN device is 3.8°C. With enhanced cooling conditions, the current sharing between paralleled devices remains within expectation.

5.3 Summary

From the measured results, it is observed that InnoGaN is suitable for parallel application., Special attentions should be paid to the symmetry in common-source inductance, power loop, and gate driving loop in the design of multi-device parallel applications. Ensuring the consistency in parasitic parameters is crucial for the reliability of paralleled InnoGaN. Additionally, for high power applications, thermal management approaches are necessary for thermal stability of the system.

6 Design Recommandation for half-bridge applications with different number of devices

Symmetry designs are crucial to for paralleled GaN devicesin common-source inductance, power loop, and gate driving loop. PCB should be designed with symmetrical structures to ensure consistency in parasitic parameters, thereby maximizing the advantages of parallel connection and enhancing system stability and reliability.

Following are several recommended parallel design examples:

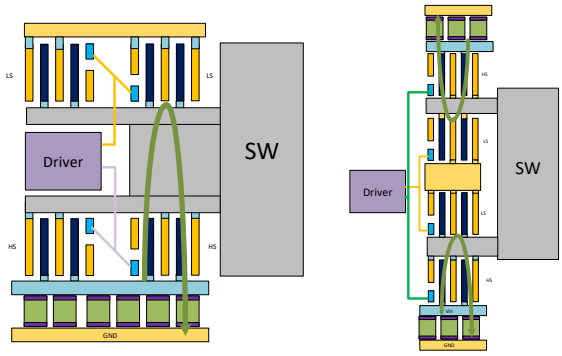


Figure 29 Design examples of 2 devices in parallel

The two design examples in Figure 29 both achieve symmetry of power loop and gate driving loop. However, the design in the left diagram is relatively campact with concentrated thermal generation compared to the right one, which needs an enhanced thermal dissipation capability and is more challenging for thermal management design.

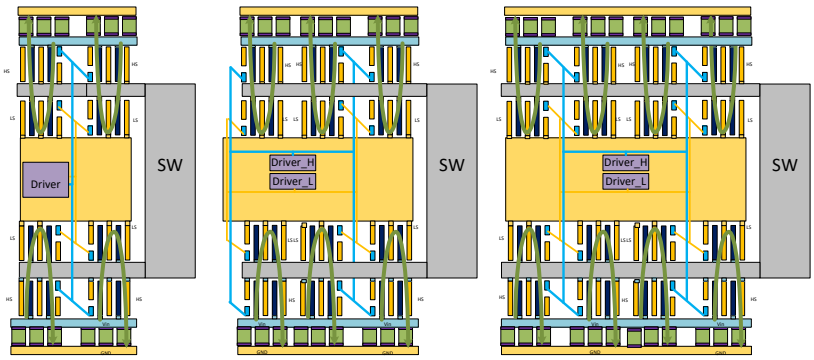


Figure 30 Design examples of 4 ~ 8 devices in parallel

The design examples of 4/6/8 devices in parallel are shown in Figure 30. Each of these designs are in symmetry of common-source inductance, power loops, and gate driving loops.

Reversion History

Date	Version	Description	Author
2024/04/28	1.0	English translation	AE team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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